CLAIMS

What is claimed is:

1. A method comprising:

entering a special programming mode of a memory that disables internal program verification by the memory, wherein the memory includes automation circuitry for program verification;

programming a plurality of words into the memory without the memory performing internal program verification;

exiting the special programming mode of the memory and enabling internal program verification by the memory.

2. The method of claim 1, further comprising having a host processor verify external to the memory the programming of the plurality of data word into the memory.

3. The method of claim 1, wherein the memory is a nonvolatile memory.

4. The method of claim 2, wherein the special programming mode is entered by the host sending a command to the memory for entering the special programming mode.

5. The method of claim 4, wherein the special programming mode is exited by the host sending a command to the memory for exiting the special programming mode.

6. The method of claim 2, wherein the special programming mode is entered by the host sending a sequence of commands to the memory for entering the special programming mode.

7. The method of claim 2, wherein the host processor sends the plurality of words to the memory for programming into the memory.

8. The method of claim 2, further comprising disabling further entry into the special program mode of the memory by sending a disable special programming mode command from the host processor to the memory.

9. The method of claim 1, wherein programming a plurality of words into the memory further comprises using only a single programming pulse for each bit of each word of the plurality of words.

10. The method of claim 1, wherein entering the special programming mode of the memory further comprises enabling a special algorithm microcoded in the memory for controlling the memory during the special programming mode.

11. The method of claim 10, wherein the special algorithm changes a length of a programming pulse to be used during the special programming mode.

12. The method of claim 2, wherein having the host processor verify external to the memory the programming of the plurality of data words into the memory comprises having the host processor read the plurality of words programmed into the memory and compare with a plurality of respective data words stored by the host processor in a second memory.

13. The method of claim 12, wherein if a word of the plurality of words read by the host processor does not compare with a respective word of the plurality of respective data words stored by the host processor in the second memory, then the host processor will (1) send the respective word to the memory for reprogramming into the memory as a reprogrammed data word without the memory performing

internal program verification, (2) read the reprogrammed data word from the memory, (3) verify external to the memory the programmed data word.

14. The method of claim 12, wherein if a word of the plurality of words read by the host processor does not compare with a respective word of the plurality of respective data words stored by the host processor in the second memory, then exiting the special programming mode of the memory and sending the respective data word to the memory for reprogramming into the memory as a reprogrammed data word with the memory performing internal program verification.

15. An apparatus comprising a memory comprising:

automation circuitry to perform internal program verification unless disabled;

special programming mode circuitry to disable internal program verification by the memory when the special programming mode circuitry is enabled.

16. The apparatus of claim 15, further comprising a host processor comprising:

circuitry to enable or disable the special programming mode circuitry of the memory;

circuitry to send to the memory a plurality of data words to be programmed into the memory without the memory performing internal program verification if the special programming mode circuitry is enabled;

circuitry to verify external do the memory programming of the plurality of data words into the memory if the special programming mode circuitry is enabled.

17. The apparatus of claim 15, wherein the memory is a nonvolatile memory.

18. The apparatus of claim 15, wherein the circuitry to enable or disable special programming mode circuitry comprises circuitry for sending special commands to the memory.

19. The apparatus of claim 16, wherein the memory further comprises circuitry to disable further entry into the special programming mode of the memory if a disable special programming mode command is sent from the host processor to the memory.

20. The apparatus of claim 15, wherein the special programming mode circuitry further comprises a special algorithm that changes a length of a programming pulse to be used if the special programming mode circuitry is enabled.

21. The apparatus of claim 16, wherein the circuitry to verify external to the memory comprises:

a second memory coupled to the host processor storing the plurality of data words;

circuitry for comparing the plurality of data words stored in the second memory with a plurality of data words read from the memory by the host processor.

22. An apparatus comprising a memory comprising:

means for performing internal program verification unless disabled;

means for disabling internal program verification by the memory upon receipt of an enablement signal.

23. The apparatus of claim 22, further comprising a host processor comprising:

means for enabling or disabling the means for disabling internal program verification by the memory;

means for sending to the memory a plurality of data words to be programmed into the memory without the memory performing internal program verification if the means for disabling internal program verification is enabled;

means for verifying external to the memory programming of the plurality of data words into the memory if the means for disabling internal program verification is enabled.

24. The apparatus of claim 22, wherein the memory is a nonvolatile memory.

25. The apparatus of claim 23, wherein the memory further comprises means for disabling further entry into the special programming mode of the memory if a disable special programming mode command is sent from the host processor to the memory.